Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application (Please note that there are no present amendments to the claims):

Listing of Claims:

Claims 1-38 (Canceled)

39. (Previously added) A method for limiting the amount of control voltage provided to an output element in an output buffer, said method comprising the steps of:

receiving a control signal in a predriver device;

providing an output voltage from said predriver device to a limiter circuit configured between said predriver device and the output element;

limiting said amount of control voltage with said limiter circuit to no greater than a maximum voltage level; and

driving the output element with control voltage.

40. (Previously added) The method according to claim 39, wherein said step of limiting said amount of control voltage comprises limiting a gate voltage provided to the output element to said maximum voltage level comprising an amount not greater than an internally regulated voltage less a threshold voltage of said limiter circuit.

41. (Previously added) The method according to claim 39, wherein said method further comprises the step of reducing a maximum current in an I-V characteristic of the output element.

42. (Previously added) The method according to claim 39, wherein said step of limiting said amount of control voltage comprises clamping said output voltage from said predriver device to an amount no greater than said maximum voltage level.

43. (Previously added) The method according to claim 42, wherein said step of limiting said amount of control voltage comprises clamping said output voltage from said predriver device based on a diode configuration of said limiter circuit configured to limit a maximum gate voltage.

44. (Previously added) The method according to claim 43, wherein said step of limiting said maximum gate voltage comprises clamping of said maximum gate voltage through at least one of a plurality of diode-connected p-channel transistors and a plurality of diode-connected n-channel transistors.

45. (Previously added) A method for controlling operation of an output buffer in a memory system, said method comprising the steps of:

receiving a control signal in a predriver device of the output buffer;

providing an output voltage from said predriver device for driving an output pull-down element of the output buffer; and

regulating said output voltage with a limiter circuit to provide a maximum gate voltage to said output pull-down element to facilitate a decrease in the size of said output pull-down element necessary for operation of the output buffer.

46. (Previously added) The method according to claim 45, wherein said step of providing said output voltage from said predriver device comprises providing said output voltage to said limiter circuit configured between said predriver device and said output pull-down element.

47. (Previously added) The method according to claim 45, wherein said step of regulating comprises clamping said output voltage with said limiter circuit.

48. (Previously added) The method according to claim 47, wherein said step of clamping said output voltage is based on a diode configuration of said limiter circuit configured to provide said maximum gate voltage.

49. (Previously added) The method according to claim 45, wherein said step of providing said output voltage from said predriver device comprises providing said output voltage to said limiter circuit configured between said predriver device and a positive supply rail.

50. (Previously added) The method according to claim 45, wherein said step of regulating said output voltage with said limiter circuit comprises limiting said maximum gate voltage provided to said output pull-down element to an amount not greater than an internally regulated voltage.

51. (Previously added) The method according to claim 50, wherein said step of regulating said output voltage with said limiter circuit comprises limiting said maximum gate voltage provided to the output element to an amount not greater than an internally regulated voltage less a threshold voltage of said limiter circuit.

52. (Previously added) A method for regulating a control voltage for an output pull-down element of an SDRAM output buffer, said method comprising the steps of:

generating an output voltage from at least one predriver device configured to control the output pull-down element of said SDRAM output buffer;

limiting said output voltage with a limiter circuit to a maximum voltage level; and

providing the control voltage to the output pull-down element, wherein said control voltage is no greater than said maximum voltage level.

53. (Previously added) The method according to claim 52, wherein said step of limiting said output voltage comprises limiting to a voltage no greater than a maximum gate voltage comprising an internally generated regulated voltage less a threshold voltage of said limiter circuit.

54. (Previously added) The method according to claim 52, wherein said step of limiting comprises limiting said output voltage through an n-channel transistor coupled to a drain of a p-channel transistor comprising said at least one predriver device.

55. (Previously added) The method according to claim 52, wherein said step of limiting comprises clamping said output voltage through a diode configuration to provide the control voltage to the output pull-down element.

56. (Previously added) A method for regulating a predriver circuit for an output buffer, said method comprising the steps of:

generating an output voltage from at least one predriver device configured to control an output element of said output buffer;

limiting said output voltage with a limiter circuit to a control voltage no greater than a maximum voltage level; and

providing said control voltage to said output element to drive said output element.

57. (Previously added) The method according to claim 56, wherein said step of generating said output voltage from said at least one predriver device comprises receiving a control signal in a predriver transistor device and providing said output voltage from a drain terminal of said predriver transistor device.

58. (Previously added) The method according to claim 57, wherein said step of limiting said output voltage comprises coupling said drain terminal to a source terminal of a transistor device configured to regulate said output voltage to provide said control voltage.

59. (Previously added) The method according to claim 56, wherein said step of limiting said output voltage comprises regulating said control voltage to an amount of voltage not greater than an internally regulated voltage less a threshold voltage of said limiter circuit.

60. (Previously added) The method according to claim 56, wherein said step of limiting said output voltage comprises clamping said output voltage to a level no greater than a maximum voltage level.

61. (Previously added) The method according to claim 60, wherein said step of clamping comprises clamping an output voltage provided from drain terminals of a p-channel predriver device and an n-channel predriver device with a series of diode devices.

62. (Previously added) The method according to claim 61, wherein said step of clamping comprises clamping an output voltage with a series of diode-connected transistors comprising at least one of a plurality of p-channel devices and a plurality of n-channel devices.

63. (Previously added) The method according to claim 57, wherein said step of limiting said output voltage comprises limiting through a limiter device comprising an n-channel transistor device an amount of voltage received by an input terminal of a p-channel predriver device.

64. (Previously added) The method according to claim 63, wherein said step of limiting said output voltage comprises regulating with said limiter device said amount of voltage

received by said input terminal of said p-channel predriver device to an amount not greater than an internally regulated voltage received at a control terminal of said limiter device less a threshold voltage of said limiter device.